REMARKS/ARGUMENTS

In view of the foregoing amendments and the following remarks, reconsideration of this application is requested. Claims 7-28 are now pending with claims 7, 11, 18, and 22 being independent. Claims 1-6 have been canceled. Amendments have been made to independent claims 7, 11, 18, and 22. No new matter has been introduced.

The Applicants gratefully acknowledge the Examiner's indication that claims 12-13 and 23-24 would be allowable if rewritten so as to include all the limitations of the respective base claims and any intervening claims. The Applicants respectfully suggest that the amendments made herein render the independent claims 7, 11, 18, and 22 similarly allowable.

Claim 7, as amended, describes a method comprising fetching and decoding instructions in a first processor, detecting an unsupported instruction that is not executable by the first processor, executing said unsupported instruction in a second processor, and providing the first processor with a supported instruction that is executable in the first processor by loading the supported instruction in decode logic of the first processor without the first processor fetching any portion of said supported instruction, **wherein the *second* processor fetches the supported instruction and loads the supported instruction in the decode logic of the *first* processor**. Claim 18, as amended, has similar recitations.

Claim 11, as amended, describes a system comprising a first processor having fetch logic and decode logic, the first processor fetches supported instructions from memory using said fetch logic and decodes said supported instructions with said decode logic, a second processor, the second processor executes unsupported instructions, means for loading a supported instruction in said decode logic of the first processor so that the first processor decodes but does not fetch any portion of the supported instruction, **wherein the *second* processor fetches the supported instruction and loads the supported instruction in the decode logic of the *first* processor**, and means for coordinating when said loading the supported instruction in said decode logic of the first processor so that the first processor decodes but does not fetch any portion of the supported instruction occurs. Claim 22, as amended, has similar recitations.

Independent claims 7, 11, 18, and 22 stand rejected under 35 U.S.C. § 103(a) as being obvious over Chung et al. (U.S. Patent No. 6,950,929). Applicants request reconsideration and

withdrawal of this rejection for at least the reason that Chung does not describe or suggest the recitation in claims 7 and 18, as amended, of providing the first processor with a supported instruction that is executable in the first processor by loading the supported instruction in decode logic of the first processor without the first processor fetching any portion of said supported instruction, **wherein the *second* processor fetches the supported instruction and loads the supported instruction in the decode logic of the *first* processor**. Chung also does not describe or suggest the recitation in claims 11 and 22, as amended, of means for loading a supported instruction in said decode logic of the first processor so that the first processor decodes but does not fetch any portion of the supported instruction, **wherein the *second* processor fetches the supported instruction and loads the supported instruction in the decode logic of the *first* processor**.

Indeed, according to the Examiner, Chung describes that "[w]hen executing a loop, **the instructions are fetched by the *first* processor** into the loop buffer during the first iteration" and that for the rest of the iterations "the instructions are sent from the loop buffer to the decoder without requiring fetching from main memory." *Office Action* mailed September 19, 2007, paragraph 7, page 3, and paragraph 11, page 5 (emphasis added). Therefore, Chung does not describe or suggest the recitation in claims 7 and 18, as amended, of providing the first processor with a supported instruction that is executable in the first processor by loading the supported instruction in decode logic of the first processor without the first processor fetching any portion of said supported instruction, **wherein the *second* processor fetches the supported instruction and loads the supported instruction in the decode logic of the *first* processor**. Chung also does not describe or suggest the recitation in claims 11 and 22, as amended, of means for loading a supported instruction in said decode logic of the first processor so that the first processor decodes but does not fetch any portion of the supported instruction, **wherein the *second* processor fetches the supported instruction and loads the supported instruction in the decode logic of the *first* processor**.

For at least the reasons given above, the Applicants respectfully submit that claims 7, 11, 18, and 22, as amended, are patentable over Chung.

Claims 8-10 depend from independent claim 7, claims 14-17 depend from independent claim 11, claims 19-21 depend from claim 18, and claims 25-28 depend from claim 22.

Accordingly, the Applicants request reconsideration and withdrawal of the rejections for claims 8-10, 14-17, 19-21, and 25-28 for the reasons discussed above with respect to claims 7, 11, 18, and 22, as amended.

In view of these remarks and amendments, the Applicants submit that this application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

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